ABSTRACT OF THE DISCLOSURE

The single-step debug card using the PCI interface according to the present invention utilizes a bus master to send out an REQ# signal to request issuing a control during the PCI bus cycle to be inspected. The address, data, command, and byte enable (BE#) of the bus cycle are locked and displayed through LEDs for single-step debugging. Through a switch circuit, a TRDY# ready signal is sent out. A device selection signal (DEVSEL#) is raised to HIGH at the same time the TRDY# ready signal finishes so as to notify the bus master on the single-step interruption debug card to end the cycle for single-step debugging.